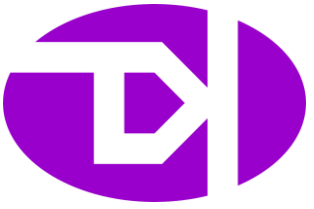


LAX016 Series Logic Analyzer User Guide

http://www.kingst.org
QQ: 415942827

Contents

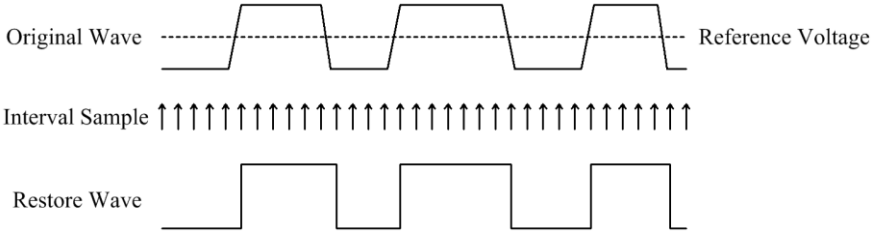
Ⅰ、 Overview

1、 Basic knowledge

Logic analyzer is the instrument that collects and displays the digital signal from the devices under test. It is mainly used for timing judgement an analysis. Unlike the oscilloscope with many voltage grades, It has only two grades(Logic one and Logic zero). .After the reference voltage is set, the logic analyzer could decide from the test signal that the signal above the reference voltage is logic one, and the signal below is logic zero. The digital waveform is formed with 1 and 0. Compared with the oscilloscope, when testing and measuring the digital systems like MCU, ARM, FPGA and DSP, the logic analyzer could provide better accuracy, much more data and more complicated measuring methods.

For example, if you are sampling a signal with the logic analyzer, the sample rate of which is 1Mhz, and the reference voltage is set to 1.5V, the logic analyzer would compare the current voltage with 1.5V. The signal above 1.5V would be high level(logic 1), and the signal below 1.5V would be low level(logic 0). Thus we get a sample point, and then we could link all these points(logic 1 and logic 0) to get a waveform, in which the user could see and analyze the timing of the signal, logic errors and the relation between each other.

The figure below shows how the logic analyzer samples the signal:



2、 Product series

This product series include LA1016、LA2016、LA5016：

3、 Technical specification

Product type		LA1016	LA2016	LA5016
Input	Total number of channels	16	16	16
	Max sample rate	100MHz	200MHz	500MHz
	Measurement bandwidth	20MHz	40MHz	80MHz
	Min pulse captured	20ns	12.5ns	6.25ns
	Hardware storage	1Gbits	1Gbits	512Mbits
	Hardware Sample depth	50M/channel	50M/ channel	32M/ channel
	Max compression depth	10G/ channel	10G/ channel	5G/ channel
	Input voltage range	-50V～+50V	-50V～+50V	-50V～+50V
	Input impedance	220KΩ, 12pF	220KΩ, 12pF	220KΩ, 12pF
	Threshold voltage	≤0.8V low level ≥1.6V high level	≤0.8V low level ≥1.6V high level	≤1.0V low level ≥2.0V high level
PWM output	Number of channels	2	2	2
	Output frequency range	0.1～20MHz	0.1～20MHz	0.1～12.5MHz
	Min interval for frequency adjustment	10ns	10ns	8ns
	Min interval for pulse width adjustment	5ns	5ns	8ns
	Output voltage	+3.3V	+3.3V	+3.3V
	Export impedance	50Ω	50Ω	50Ω
power supply	Power supply port	USB2.0/3.0	USB2.0/3.0	USB2.0/3.0
	Standby current	130mA	150mA	300mA
	Maximum active current	260mA	300mA	550mA
PC software	Supported protocols	UART(RS-232/485/422)、I2C、SPI、CAN、DMX512、I2S/PCM、Manchester、1-Wire、Simple Parallel、UNI/O		
	Supported OS	Windows XP、Vista、Windows 7/8(32bit/64bit)		

II、 Brief introduction to JkiSuite software

1、 How to install the software

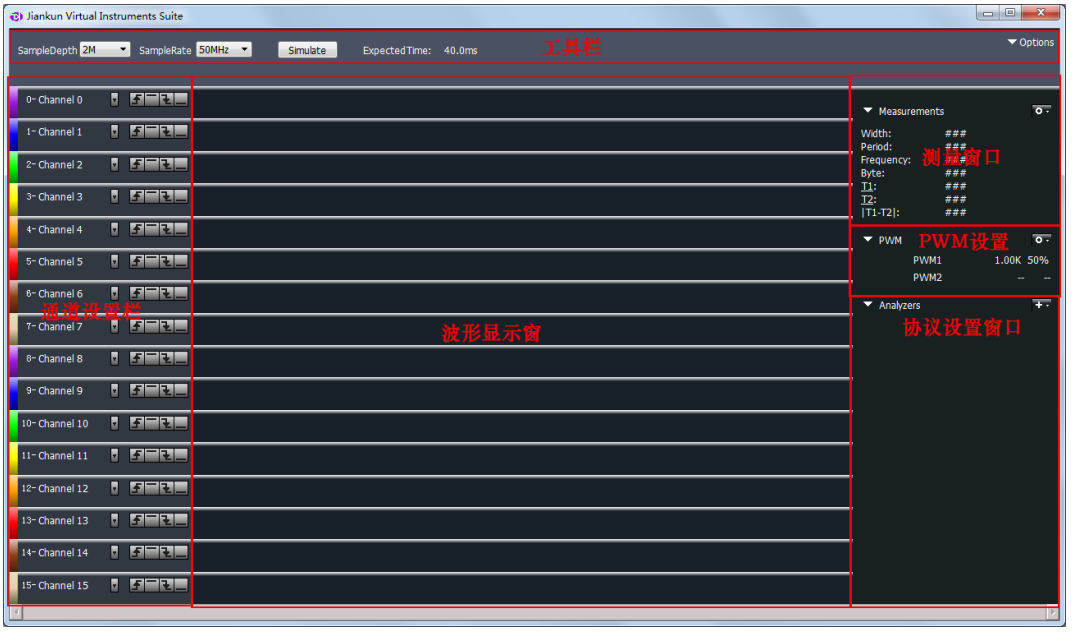
The software package is JkiSuiteSetup.exe. and it could be found in the attached CD, or downloaded from the link: http://www.kingst.org/download?fl=JkiSuiteSetup.zip,

Double click “JkiSuiteSetup.exe” to execute the installation program. The procedure is similar with the common software in windows, and there are instructions that you could follow in every step. In the last step, you should install the driver program of hardware device, and you will see the dialog as the figure below(there could be differences between different OSs). Please select “Install” to complete the procedure.

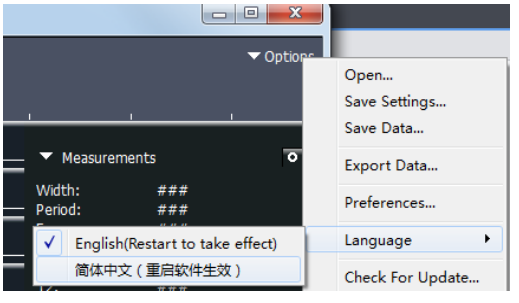
After the install procedure is complete, a shortcut like  would be created in the start menu and desktop, and then the JkiSuite software could be accessed with this shortcut.

2、 Brief introduction to GUI

Whe the software is started through start menu or desktop shortcut, you will get a screen similar to the figure below. It contains the tool bar, channel settings bar, waveform display window, measurement window, PWM settings window and analyzers settings window.

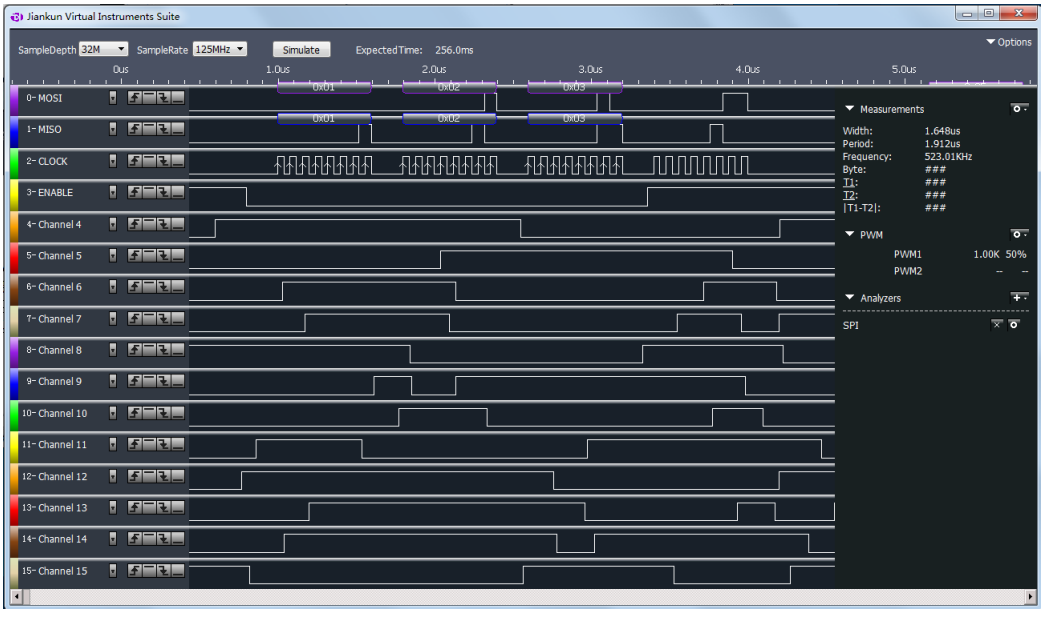


The software could display in “English/简体中文”. If you want to change the language, you could press the “Optios” button in the top right corner, and select the language. The selection would become effective after the software is restarted.



3、 Brief introduction to the demo function

The software could provide demo function. You can simulate the functions without the actual hardware, and you could get a good experience of the software through this function. With the example of SPI, you could press the “+” button on the right side of “Analyzers” In analyzers settings window, the SPI analyzer would be added with default configurations. Then you could set sample depth and sample rate, and the sample time would be calculated automatically by the software. After all these are done, just press the “Simulate” button in the tool bar and you will get simulation waveform, which is shown in the figure below.



In the figure above, channels 0-3 contain the simulated SPI signals, and the signals in other channels are random. You could zoom the waveform though the mouse, and if you click the left button without releasing, you could drag the waveform. More details are covered in following chapters.

III、 Connect the device

1、 Connect the device to PC

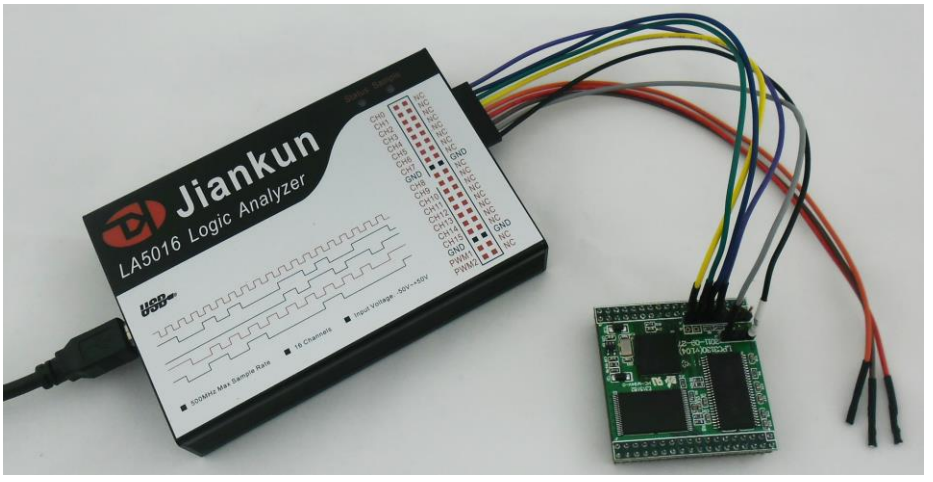
When the installation process is completed, the logic analyzer can be connected to PC through the attached USB cable (In case of desktop computer, use the USB port behind the tower box). Then the computer would report that new hardware has been found. In Windows XP, there would appear a driver installation dialog, and just select to install automatically. In Windows 7/8, a dialog would appear in the top right corner of the screen. Then the install process would start automatically, and we just need to wait for a while. After the installation process is completed, a new device called “Jiankun Instrument-Logic Analyzer” would appear in “Device Manager->Universal Serial Bus”.

2、 Connect device to system under test

Please note that the logic analyzer and the computer share the same ground, so the voltage between the GND of system under test and the CND of the computer should be zero. Especially when the system is connected to the force electricity, please make sure the isolation is made. If devices with force electricity like frequency transformer are not isolated through the isolation transformer, the system would be connected to the force electricity. And if you connect the logic analyzer to such a system, the logic analyzer even the computer would be broken. And the damage could be beyond repair, so the isolation should be made in advance.

When the logic analyzer is connected with the system under test, you should first connect the GND channel to the system under test, and then connect the signal channels. There are 16 channels in the logic analyzer. It means that up to 16 digital signals could be tested simultaneously. If the number of existing signal is less than 16, the channels could be selected at will. The channel numbers of the software correspond to that of the hardware device.

In addition, when measuring the signal with high speed, the measuring lines of logic analyzer should be near the signal of system under test. The cable between the logic analyzer and the system under test should not be long, because long cables would result in heavy inductive effect and signal reflection. Therefore it is recommended that in debug stage of the system some pins should be reserved on the experiment board to make the best of measurement. The connection between the logic analyzer and the system under test is shown in the figure below:



3、 Multipoint grounding to increase accuracy

when measuring multiple channels with high frequency signal, the signal current from all channels would flow into the system under test through GND channel, and the inductive effect of the wire in high frequency is strong, so signal current of multiple channels would overlap on GND channel, and as a result of that, the instantaneous voltage difference would be too large to result in the "glitch" on the waveform under test.

To remove these "glitches", we could take the multipoint grounding method. Normally the logic analyzer would provide several GND channels. If we connect these channels to the grounding point of the system under test, the signal current which we have mentioned would be divided into different path, and the "glitch" could also be removed. The multipoint grounding mainly includes:

Direct connection——GND channel of the logic analyzer should be connected to the GND wire of the system under test directly.

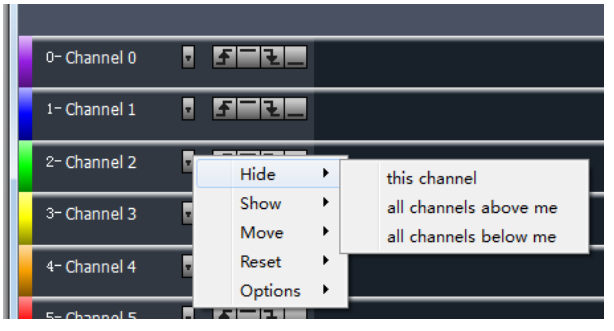
Dispersed connection——the GND channels should be connected to different parts of the system under test. Multiple GND channels should not be connected to one grounding point of the system.

Ⅳ、 Details of operations

After the software installation and device connection are complete, we could sample the signal and analyze it. In this chapter we will see how to use the logic analyzer step by step. Some of these steps need to be configured only once, and in future operations we could just skip them.

1、 通道设置 Channel settings

There are 16 channels in the logic analyzer, and not all these channels would be in real use. Limited to the size of computer screen, when more channels need to be displayed on the screen, every channel looks even smaller, and it is not convenient to watch. After setting some parameters, the software could display the channels required, and hide other unused channels. We can make it done in this way: Press the down arrow on the right side of the channel label, and select “Hide” or “Show” to hide or show the channel. As shown in the figure below, the settings could be used for “this channel”, “all channels above this channel ” and “all channels below this channel”.



In addition, current channel could be moved up and down through the “Move” menu. “Reset” menu will restore the channels to default settings and labels, and “Options” menu could hide or show the trigger button bar and channel label bar.

2、 Sample depth and sample rate

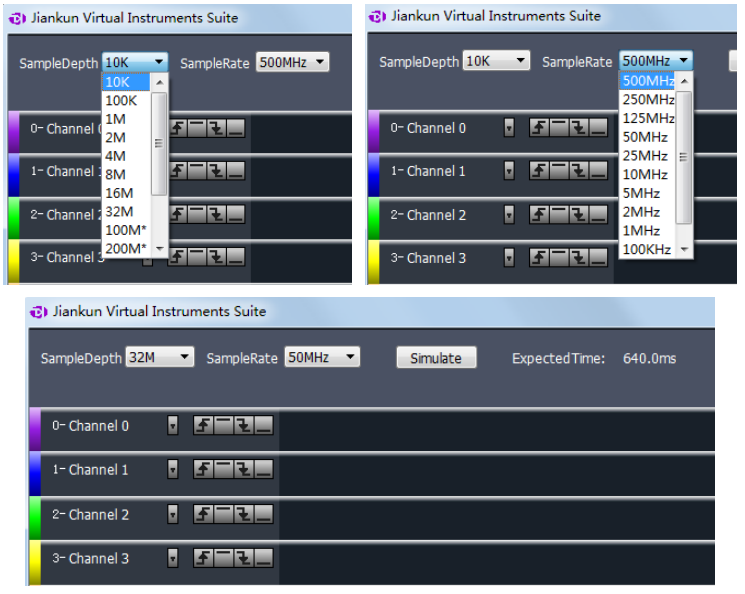
Sample depth is the number of sample points. It determines how much data the logic analyzer could sample at a time. And it is apparent that the larger sample depth is, the more data it could sample.

Sample rate, the frequency to sample the signal, is the number of sample point per second. It determines the time accuracy of sample result. Larger sample rate results in better accuracy. The sample period represents the time accuracy of sample result.

The time one sampling process could last equals to “sample depth÷sample rate”. Before sampling, we could first estimate the signal to test about the maximum frequency, the data required, etc. Then we could select the sample rate based on the maximum frequency, and we might follow the following rule: Sample rate should be 5 times more than the signal to test,

and 10 times would be better. However, it is not a good idea to have a too large sample rate, because with the same sample depth, large sample rate means short sample time. Therefore, sample rate and sample time are two factors we should consider. In real applications, the parameters should be slightly more than the minimum requirement.

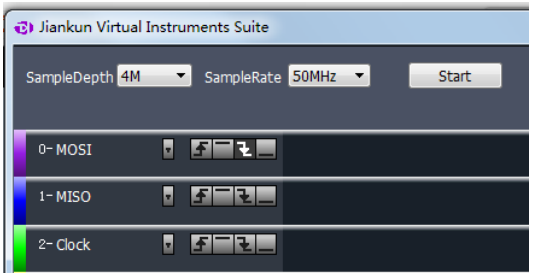
The settings of sample depth and sample rate are shown in the figure below:



3、 Set trigger conditions

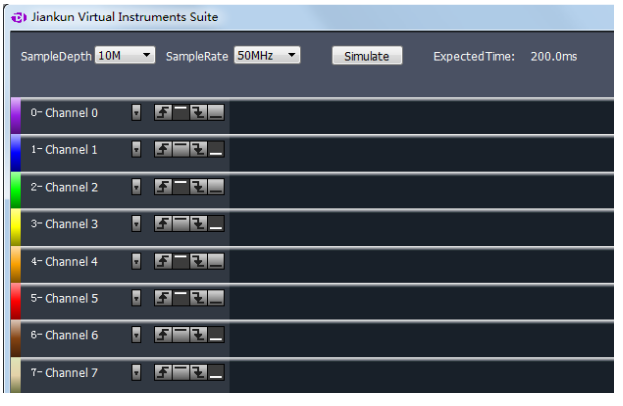
In the example above, the logic analyzer could sample signal of 640ms with 32M sample depth and 50M sample rate. The trigger is not set by default, and if we press “start” button, the logic analyzer would start to sample. It would stop automatically in 640ms, and display the waveform in the screen. But in real environment, the signal may not be continuous, and the user can not tell when it would occur, such as UART communication. In this way, maybe we could not sample any effective data during the time since we pressed “start”. To solve this problem, we could utilize the trigger function.

First we set a certain condition, and then when the signal meets the condition, the data sample would start. This is how trigger works, and the conditions here are trigger conditions, such as jump edge of the signal, high/low level or the combinations of them. The trigger conditions should be set based on the characteristics of the signal to test, for example, in UART communication, for the idle state in which no data are transferred, the signal is high level, and every UART data frame is started by the transfer from idle state to start bit, which is low level, so we should set the falling edge of this channel as the trigger condition. If the channel 0 is used for UART signal, we just need to press the “falling edge” button on the right side of channel 0.



After the trigger is set and the button “start” is pressed again, if the trigger condition (falling edge) we have set have not appeared on channel 0, the logic analyzer would stay in wait state until the falling edge arrives. Then the device will sample and save the data, and upload the data to the computer for displaying and analyzing when the process is complete.

Except the edge and level trigger condition for single channel, the logic analyzer also supports the condition combinations of multiple channels, such as levels, one edge and multiple levels. The final condition is the “logical AND” of these conditions, which means the sampling process starts when all conditions are met. In this way, the trigger can be the result of certain parallel data. It could be used in the situation when the master device like MCU accesses the peripheral through the bus and we want to check the data write/read operations of a certain address. For example, if we want to check the data operations of address 0x35, channels 0-7 should be connected to 8 address lines, and the other channels are connected to the data lines. After we set the level combination of channel 0-7 as the trigger condition, the data in this address could be sampled. The trigger settings are:

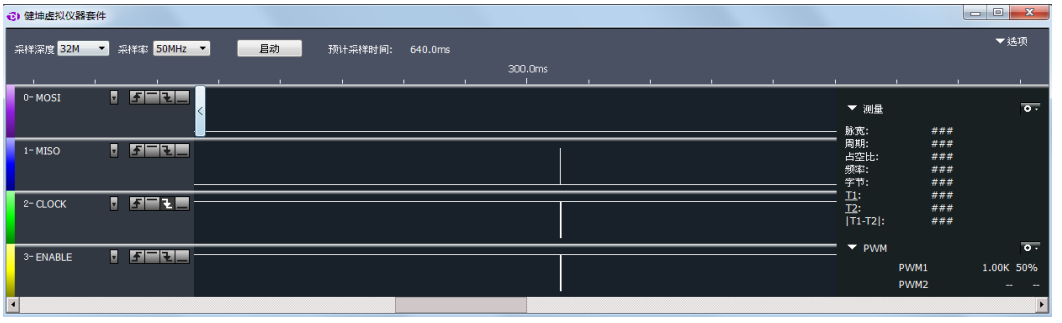


4、 Get the waveform

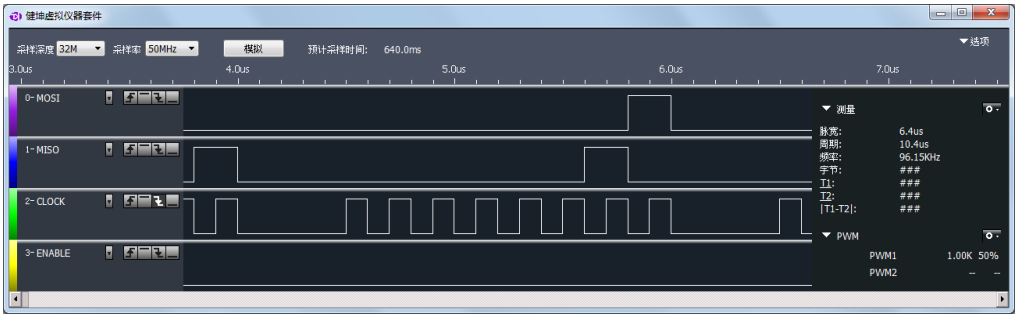
The sampling process is started by pressing the “start” button. The logic analyzer samples the signal since then (trigger conditions should be met if they are set), and stops if it has got the sample points (sample depth) required. It would upload the data to the computer. The software would restore the waveform and maybe measures or analyzes the data later.

5、 Check and measure the waveform

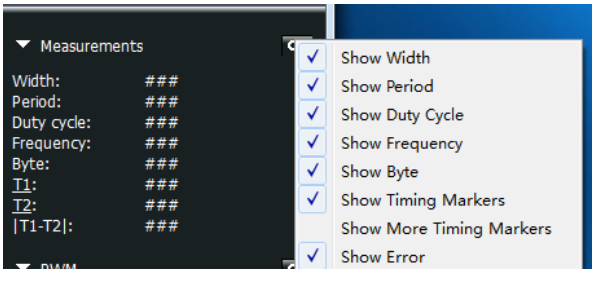
After the sampling process is complete, the waveform would be displayed in the screen.



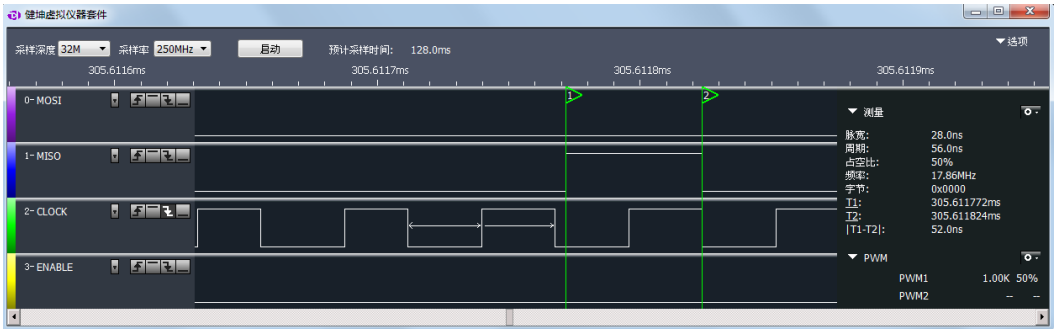
From this figure, we can see the coordinate values of the time axis are too large, and the effective waveform is within a very short period. You can click the left button of the mouse to zoom out the waveform; while the right button would zoom it in. And you can get these done with the mouse wheel too. After the waveform is zoomed up, you could s ee:



From the measurement window, we can see the relative data of current waveform. And all the measurement items could be turned on or off by pressing the circle on the right side of the measurement window.



After the measurement items required are set, if you move the mouse to the waveform window, the software would measure the relative data of the position where the cursor stays, and display them in the measurement window.

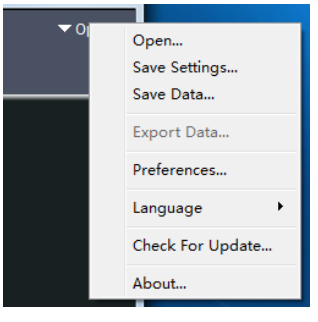


For example, if the cursor is located in the low pulse of channel 2, an arrow would appear in the high pulse next to this pulse. And at the same time, the relative measurement information would appear in the measurement window on the right side. Pulse width which is 28ns refers to the low level pulse, and the period is result of low level + next high level, which is 56ns. The duty cycle is 50%, and the frequency is 17.86MHz. The byte is a 16-bit data which is the combination of value in channel 15-0.

When we press the T1 and T2 in the measurement window, a vertical green line which is called time marker would appear. If we press T1 and put the marker on the rising edge of channel 1, then we press T2 and put the marker on the falling edge of channel 1, the time corresponding to T1 and T2 would appear on the right side, and the absolute value of time difference between T1 and T2 would also be calculated. In addition, there is another time marker T3, which can be turned on through the options menu of measurement window, and provide more information.

6、 Data save and export

The data sampled could be saved into the hard disk of the computer for future check and comparison. Data saving can be handled through the menu “options->save data” on the top right corner of software interface. You just need to specify the file path and file name to save. If you need to check the data saved before, just use the menu “options->open”.

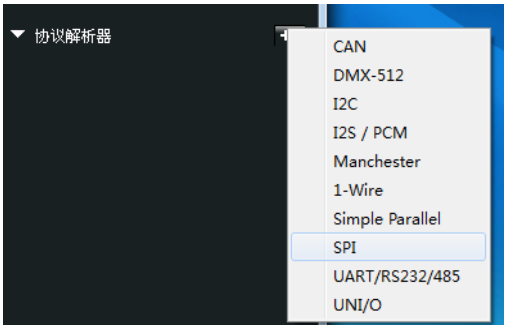


Instead of the sample data, the menu “save settings” only saves the configuration data. “Export data” could export sample data in the format of txt, bin and csv, and they could be used in other software like MATLAB, Excel.

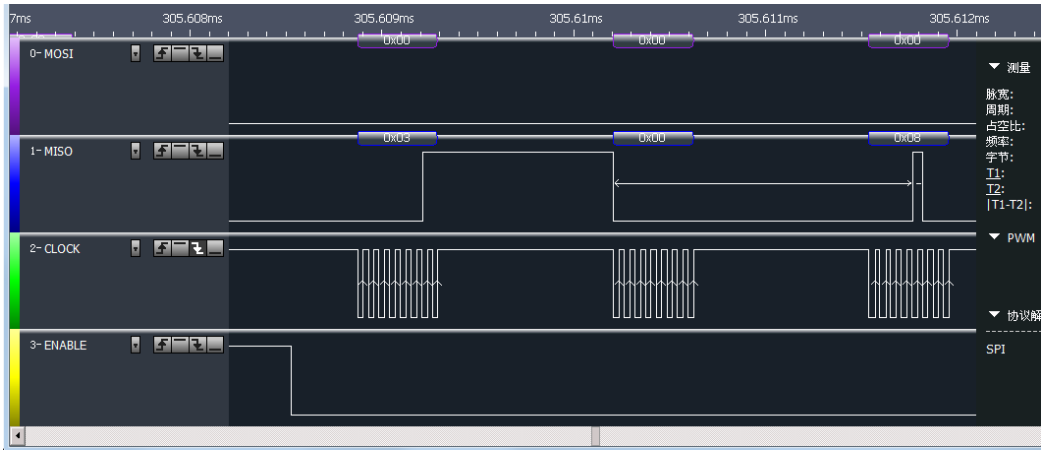
7、 Analyze standard protocols

If the signal to test conforms to standard protocols like UART, I2C, SPI which are supported by JkiSuite software(the complete protocol list is in section “Product technical specification”), besides displaying the waveform and some measurement data, the software could analyze the data to get the specific data according to protocol specifications.

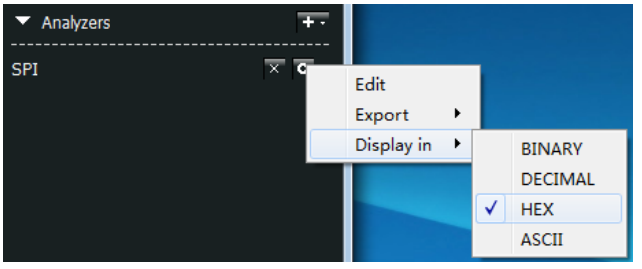
For example, channels 0-3 are used for the standard 4-wire SPI signal. You can press the “+” button on the right side of the analyzers window and select SPI in the dialog.



In this dialog, the actual parameter of SPI should be set (Please check section “Standard protocol set” for more details). When this is done, the SPI analyzer would be added. Then the software would analyze the data of channels 0-3 according to standard SPI timing specification, and display the result on channel MOSI and channel MISO.

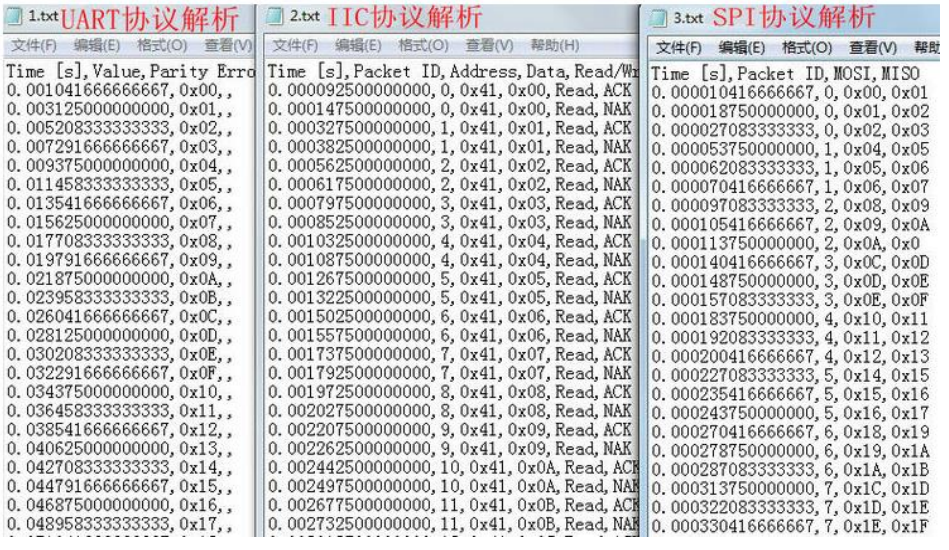


The data is displayed in hexadecimal by default. If you want to change the format, please press the button which looks like a circle in the analyzer bar, and select the format required in the menu.



The analyzed data could be exported as txt or csv through “export” menu, and they could be used in other software. If you want to change the configuration of SPI analyzer, the menu “edit” could provide help. “×” button on the left could remove the analyzer.

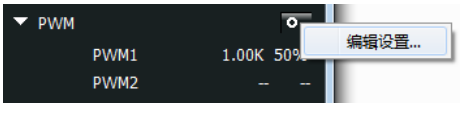
The figure below shows the exported data of UART, I2C and SPI, and we can see the result contains time value, data packet number and the analyzed data.



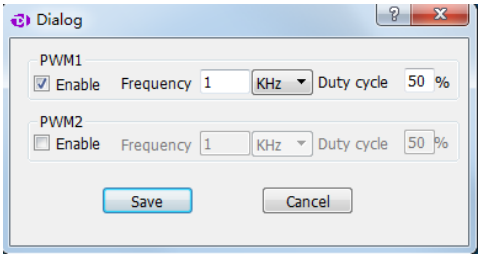
8、 PWM export

There are two PWM waveform generators in the logic analyzer, and they can generate square wave whose duty cycle could be adjusted. By default, PWM1 is turned on, and outputs 1KHz square wave with 50% duty cycle; while PWM2 is turned off, and outputs low level.

As is shown in the figure below, the PWM settings could be change through the menu button on the right side of PWM settings window.



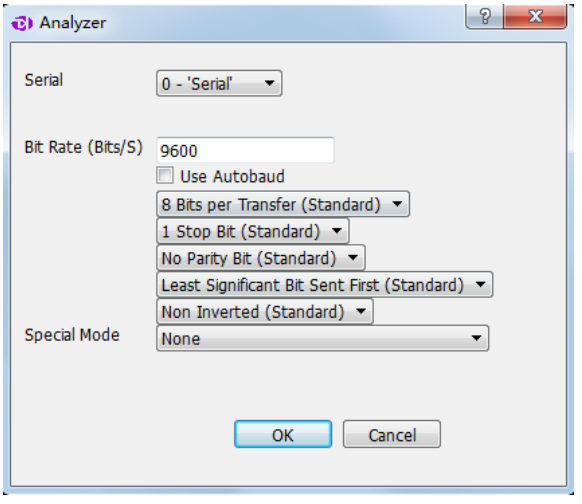
In this dialog, the PWM channel could be turned off through “Enable” box. If it is turned on, we could edit the frequency and duty cycle. After the settings are complete, just press the “save” button, and the software will generate the PWM signal with the new configuration.


Dialog
PWM1
Enable
Frequency
1
KHz
Duty cycle
50
%
PWM2
Enable
Frequency
1
KHz
Duty cycle
50
%
Save
Cancel

Ⅴ、 Settings for standard protocols

1、 UART/RS232/485

For standard UART, RS232 and RS485, they have the same timing definitions of the physical layer, so they share the same analyzer, and the figure below shows the setting dialog of UART/RS232/485 analyzer.



1st item, select the channel to use.

2nd item, set the baud rate, and the baud rate here should match that in actual use.

3rd item, use the auto baud, and the software could identify the baud rate automatically. In case of the baud rate is unknown, this option should be enabled. But the accuracy of automatic identification depends on actual signal, and the result could be incorrect.

4th item, select the number of data bits, and it is 8 most of the time.

5th item, select the number of stop bits, and there are 3 options: 1, 1.5 and 2.

6th item, set the parity bit, and there are 3 options: no parity, even parity and odd parity..

7th item, set the bit order in data transfer, and the options could be LSB(Least Significant Bit Sent First) and MSB(Most Significant Bit Sent First).

8th item, invert the data or not. Normally Inverted is only used for RS232(As For RS232, positive level is 0 and negative level is 1) and Non Inverted could used for UART and RS485.

9th item, set bit 9 as address flag in multiple machine communication or not, and by default, None. When this mode is actually used (seldom used, note that it is different with RS485 multiple machine communication), it could be used for address byte flag.

Please note that if the signal under test is differential signal like RS485 and RS232, there are 3 ways to connect the wire:

① The GND channel of the logic analyzer is connected to the GND of the test system, and 2 signal channels are connected to RXD and TXD pins of the level shift chip respectively .

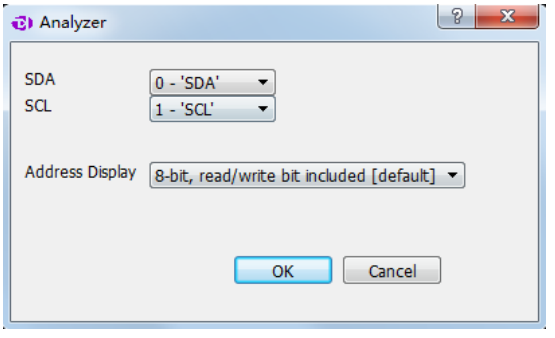
② The GND channel of the logic analyzer is connected to the GND of the test system, and 1 signal channel is connected to the A end of the RS485 bus.

③ Connect the RS485 bus to a module that transfer RS485 to TTL, and the GND and a signal channel of the logic analyzer are connected to the GND and signal export end of the system under test.

Most of the time, all these 3 ways could be used to sample the signal, but according to RS485 specification, the voltage which the AB ends could identify is between 0.2～6V. In complicated situations, such as master with many slaves or long wire, the difference of the bus end could be too little, and the logic analyzer could not identify the signal level correctly with method 2. So method 1 and method 3 are recommended if conditions permit.

2、 I2C

The setting dialog of I2C analyzer is shown below:



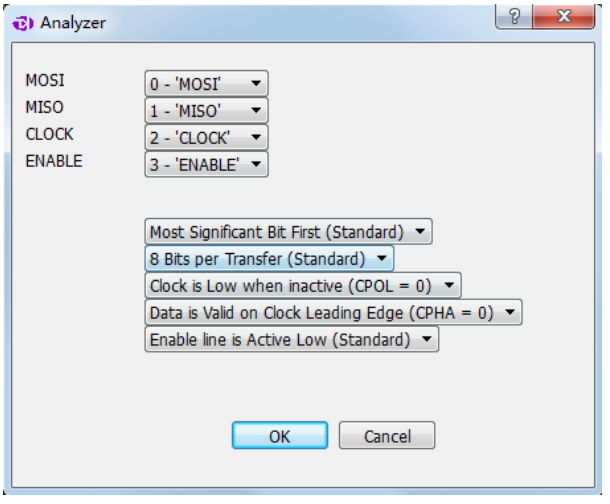
1st item, the channel used for SDA signal (data)

2nd item, the channel used for SCL signal (clock)

3rd item, the way to display the address byte. For I2C protocol, every communication is started with addressing operation, and this byte contains 1-bit read/write flag and device address which is 7-bit wide. And there are three options to display: to display as a whole (8-bit, read/write bit included); to display as a whole but the read/write flag is 0(8-bit, read/write bit set as 0); only display 7-bit address (7-bit, address bits only).

3、 SPI

The setting dialog of SPI analyzer is shown below:



1st item, the channel for MOSI signal(master out slave in)

2nd item, the channel for MISO signal(master in slave out)

3rd item, the channel for CLOCK signal(clock)

4th item, the channel for ENABLE signal(enable)

5th item, transmission mode of data bits: MSB(Most Significant Bit First) or LSB(Least Significant Bit First), usually MSB.

6th item, data length for one transfer, usually 8 or 16 bits.

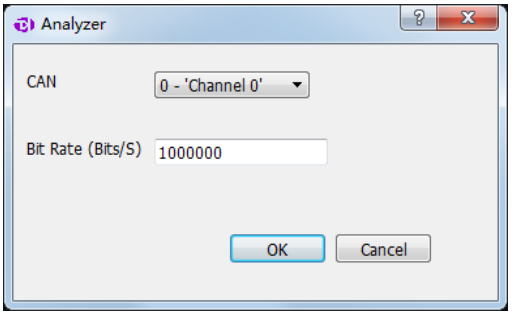
7th item, idle state of the clock. CPOL = 0: the clock wire remains low in idle state. CPOL = 1: the clock wire remains high in idle state.

8th item, the edge in which data is latched. CPHA=0: data latched in last clock edge. CPHA=1: data latched in next clock edge.

9th item, the active level of enable signal: active low(Enable line is Active Low) or active high(Enable line is Active High).

4、 CAN

The setting dialog of CAN analyzer is shown below:



1st item, the channel to use.

2nd item, baud rate in communication.

Please note that the signal from CAN bus is differential, there are 3 ways to measure CAN signal:

① The GND channel of the logic analyzer is connected to the GND of the test system, and 2 signal channels are connected to RXD and TXD pins of the level shift chip respectively.

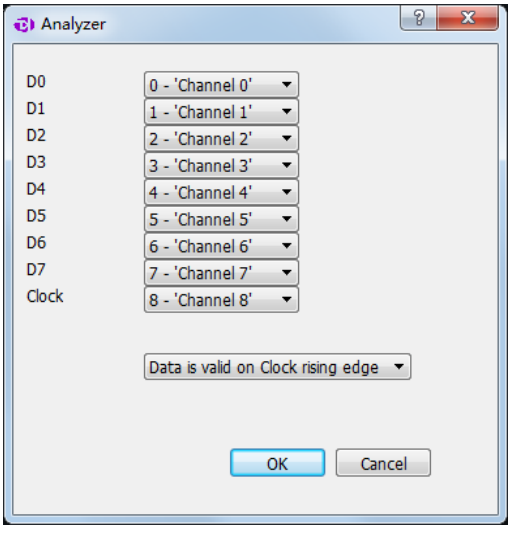
② The GND channel of the logic analyzer is connected to the L end of CAN bus, and 1 signal channel is connected to the H end of CAN bus.

③ Connect the CAN bus to a module that transfer CAN to TTL, and the GND and a signal channel of the logic analyzer are connected to the GND and signal export end of the system under test.

Most of the time, all these 3 ways could be used to sample the signal, but according to CAN specification, the voltage between the H-L ends is 0V and 2V. In complicated situations, such as master with many slaves or long wire, the difference of the bus end could be too little, and the logic analyzer could not identify the signal level correctly with method 2. In addition, the GND channel of method 2 need to be connected to the CAN-L end, but if other signals need to be tested at the same time, the grounding could be confusing. So method 1 and method 3 are recommended if conditions permit.

5、 Simple Parallel

The setting dialog of simple parallel analyzer is shown below:



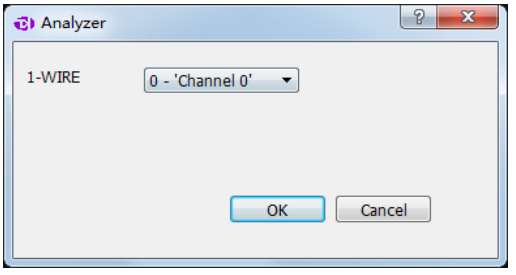
1st~8th item, the channel used for data bus.

9th item. the channel used for clock signal of data latch.

10th item, data latch on the rising edge(Data is valid on Clock rising edge) of clock signal or falling edge(Data is valid on Clock falling edge).

6、 1-Wire

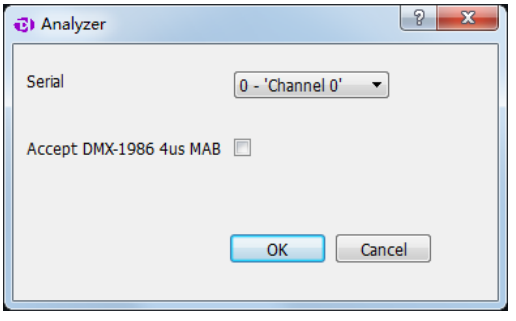
The setting dialog of 1-Wire analyzer is shown below:



1st item, the channel to use.

7、 DMX-512

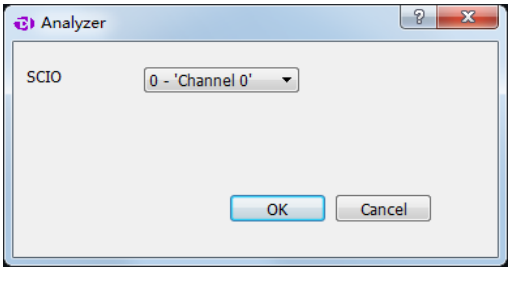
The setting dialog of DMX-512 analyzer is shown below:



1st item, the channel to use.
2nd item, accecpt DMX-1986 4us MAB signal or not.

8、 UNI/O

The setting dialog of UNI/Oanalyzer is shown below



1st item, the channel to use.

9、 User-defined protocol analyzer

Besides the standard protocol analyzers in the software, the API functions provided by the software allow users develop their own analyzers. The software API and user manual could be downloaded from the link below:

http://www.kingst.org/download?fl=JkiAnalyzerSDK.zip

VI、 FAQs

1、 Driver installation fail with the device connected to computer

First, JkiSuite should have been installed before connecting the device to computer. If the software has not been installed, the OS could not find the driver, so the installation would fail. And it would be a good idea to install the software without the hardware connected to the computer.

Second, the device driver is installed automatically by installation program during installing process. If the driver installation is blocked unintentionally during installation process, or it is not installed correctly due to other reasons, when you connect the device for the first time, the driver installation would fail too. In this case, you can find the unknown hardware devices in the device manager, click the right button to install the driver program again. Please select manual installation. The driver program is located in "installation directory\Drivers", and select the right directory based on your operating system.

2、 Identification fail or work unstably with the device connected to the computer

When the logic analyzer works at full speed, there would be a lot of the current consumed (maybe more than 500mA). So if the USB port of the computer can not supply sufficient power, the device could be identified incorrectly or work unstably. To solve this, the laptop users could try to switch to the USB port on the other side, and the desktop users must use the USB port behind the tower box. If the USB-HUB is being used, please connect the device USB port directly.

3、 Signal glitches appear on individual channels

There are two cases when signal glitches appear: the unused channels are floating, or several signals with high speed are sampled simultaneously.

It is normal that the glitch appears on unused channels, this is because the floating channel wire is like an antenna, and it will transmit weak and alternating signal, and this would result in glitches. We could hide such channels, or keep them and the signal channels at a longer distance. And we should check the grounding of the logic analyzer and the system under test.

And for the glitches which appear when measuring multiple channels with high speed, the reason for that has been explained in the section "Multipoint grounding to increase accuracy", and the method to handle this is multipoint grounding

4、 The actual sample time is less than expected when the depth is set to a large value

The logic analyzer is designed with a large-sized memory, to store the sample data temporarily. And through compression algorithm the depth is further extended. With this compression algorithm, the current and last sample data would be compared, if they are not the same, a new sample data would be generated; otherwise, only the count for last state would be incremented and no new sample data would be generated. And as a result of this, if the signal is discontinuous (for most communication system) or change slowly, the sample depth would be extended greatly. However, if the signal change rapidly the extension effect would not be so obvious. This is why the sample time is less than expected when the sample depth is set above 100M (all the depth items with *) and the signal changes rapidly.

5、 Auto update of the software fails

The software supports auto update, when a new version is released, a message would tell the user to update. However, because of system permission and security policy of the operating system, the auto update could fail. It this happens, the user could download the software from our website, and after uninstalling the software, the user could install the new version.

http://www.kingst.org/download?fl=JkiSuiteSetup.zip

VII、 contact us

Thanks for choosing our product, if you have any questions, please contact us in the following ways, and we will serve you wholeheartedly.

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Web：http://www.kingst.org

E-mail：51kingst@163.com

QQ：415942827